Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended):

A memory translation hub comprising:

a memory bus interface that provides a memory bus having a memory bus cycle time;

a memory channel interface that receives a memory control packet from a memory channel that times transmission of the memory control packet based on the memory bus cycle ~~time;~~ time, wherein the memory control packet includes command flag bits that indicate that the memory control packet is one of an activate command, a read/write command, and an extended command, the command flag bits being the first bits in the memory control packet; and

a command generator coupled to the memory channel interface and to the memory bus interface, the command generator causing the memory bus interface to provide memory control signals on the memory bus responsive to the memory control packet.

2. (original):

The memory translation hub of claim 1 wherein the memory channel includes a control portion and a data portion, the memory channel interface receiving a memory control packet only from the control portion of the memory channel.

3. (cancelled)

4. (original):

The memory translation hub of claim 3 wherein the memory control packet specifies a memory row, a memory row address, a memory bank address, and a device identification mask if the memory control packet is the activate command.

5. (original):

The memory translation hub of claim 3 wherein the memory control packet specifies a memory row, a memory column address, and a memory bank address, if the memory control packet is the read/write command.

6. (original):

The memory translation hub of claim 3 wherein, if the memory control packet is the extended command, the memory control packet includes extended flag bits that indicate that the memory control packet is one of a retire with mask command, a pre-charge command, and a service command.

7. (original):

The memory translation hub of claim 6 wherein the memory control packet specifies a memory row, and a byte mask, if the memory control packet is the retire with mask command.

8. (original):

The memory translation hub of claim 6 wherein the memory control packet specifies a memory row, and one of a broadcast flag and a memory bank address, if the memory control packet is the pre-charge command.

9. (original):

The memory translation hub of claim 6 wherein the memory control packet specifies a memory row, an operation, and one of a broadcast flag and a memory bank address, if the memory control packet is the service command.

10. (original):

The memory translation hub of claim 9 wherein the operation is one of a no operation, refresh, self refresh entry, self refresh exit, power-down entry, power-down exit, clock stop, current calibrate and sample, and temperature calibrate.

11. (original):

The memory translation hub of claim 2 further comprising a write logic circuit coupled to the memory channel interface and to the memory bus interface, the write logic circuit receiving a write data packet from the memory channel interface and causing the memory bus interface to provide memory control signals and data signals on the memory bus responsive to the write data packet, the memory channel interface receiving a write data packet only from the data portion of the memory channel.

12. (original):

The memory translation hub of claim 2 further comprising a read logic circuit coupled to the memory channel interface and to the memory bus interface, the read logic circuit receiving read data from the memory bus interface, generating a read data packet containing the read data, and causing the memory channel interface to transmit the read data packet on the data portion of the memory channel.

13. (currently amended):

A memory translation hub comprising:

means for receiving a memory control packet from a memory channel with a timing based on a cycle timing of a memory ~~bus;~~ bus, wherein the memory control packet includes command flag bits that indicate that the memory control packet is one of an activate command, a read/write command, and an extended command, the command flag bits being the first bits in the memory control packet;

means for translating the memory control packet to memory control signals; and

means for generating the memory control signals on the memory bus.

14. (original):

The memory translation hub of claim 13 wherein the means for receiving a memory control packet further comprises means for receiving a memory control packet from a control portion of the memory channel responsive to the memory control packet.

15. (original):

The memory translation hub of claim 14 further comprising:

means for receiving a write data packet from a data portion of the memory channel;

means for providing memory control signals and data signals on the memory bus responsive to the write data packet.

16. (original):

The memory translation hub of claim 14 further comprising:

means for receiving read data from the memory bus;

means for generating a read data packet containing the read data; and

means for transmitting the read data packet on a data portion of the memory channel.

17. (currently amended):

A method of connecting a memory bus to a memory controller hub through a memory channel comprising:

receiving a memory control packet from the memory channel, timing of receiving the memory control packet being based on a cycle timing of the memory ~~bus;~~ bus, wherein the memory control packet includes command flag bits that indicate that the memory control packet is one of an activate command, a read/write command, and an extended command, the command flag bits being the first bits in the memory control packet;

translating the memory control packet to memory control signals; and

generating the memory control signals on the memory bus.

18. (original):

The method of claim 17 further comprising:

receiving a write data packet from the memory channel; and

providing memory control signals and data signals on the memory bus responsive to the write data packet.

19. (original):

The method of claim 17 further comprising:

receiving read data from the memory bus interface;

generating a read data packet containing the read data; and

transmitting the read data packet on the memory channel.

20. (currently amended):

A memory subsystem comprising:

~~a memory control hub;~~

~~a memory channel coupled to the memory control hub;~~

a memory ~~bus;~~ bus having a memory bus cycle time;

a memory device coupled to the memory bus; ~~and~~

a memory channel;

a memory control hub coupled to the memory channel, the memory control hub transmitting memory control packets based on the memory bus cycle time, wherein memory control packets include command flag bits that indicate that each of the memory control packets is one of an activate command, a read/write command, and an extended command, the command flag bits being the first bits in each of the memory control packets; and

a memory translation hub coupled to the memory channel and to the memory bus, the memory translation hub to receive a memory control packet from the memory channel, and to generate memory control signals on the memory bus responsive to the memory control packet.

21. (original):

The memory subsystem of claim 20 wherein the memory channel includes a control portion and a data portion, the memory translation hub receiving a memory control packet only from the control portion of the memory channel.

22. (original):

The memory subsystem of claim 21 wherein the memory translation hub further receives a write data packet from the data portion of the memory channel, and generates memory control signals and data signals on the memory bus responsive to the write data packet.

23. (original):

The memory translation hub of claim 21 wherein the memory translation hub further receives read data from the memory bus interface, generates a read data packet containing the read data, and transmits the read data packet on the data portion of the memory channel.